HOLT INTEGRATED CIRCUITS INC.

HI-1592

Radiation-Hard MIL-STD-1553 3.3V Dual Transceiver

August 2024

DESCRIPTION

The HI-1592 is a radiation-hardened, hermetically packaged MIL-STD-1553 dual transceiver designed for use in high reliability MIL-STD-1553 applications, such as launch vehicles, high altitude aircraft and space. As aircraft fly at higher altitudes or in space they become more susceptible to exposure to cosmic rays, resulting in effects such as single-event transient (SET), single-event functional interrupt (SEFI), single event latch-up (SEL) and single event burnout (SEB), any of which could result in degradation or failure of electronic equipment. To that end, electronic equipment designed to fly in these environments needs some level of latch-up immunity or radiation hardness assurance (RHA) against the effects of cosmic rays.

The HI-1592 is designed to provide latch-up immunity up to an LET of 67.7 MeV-cm^2/mg and an RHA total ionizing dose (TID) of 100 krad(Si). It is ideal for launch vehicle and high-altitude aircraft applications utilizing MIL-STD-1553 data bus communication.

The device also features 1.8V, 2.5V and 3.3V compatible digital I/O, making it easier to interface with a broader range of FPGAs and controllers.

The transmitter takes complementary CMOS / TTL Manchester II bi-phase data and converts it to differential voltages suitable for driving the bus isolation transformer. Separate transmitter inhibit control signals are provided for each bus. The receiver section of the each bus converts the 1553 bus bi-phase analog signals to complementary CMOS / TTL data suitable for input to a Manchester decoder. Each receiver has a separate enable input, which forces the receiver outputs to the bus idle state (logic "0") when low.

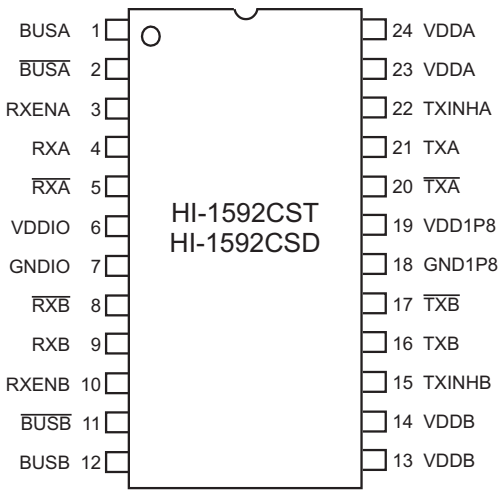
APPLICATIONS

- Launch Vehicles
- High altitude aircraft MIL-STD-1553 Terminals
- Low-orbit satellites
- Flight Control and Monitoring
- ECCM Interfaces
- Radar Systems

FEATURES

- Robust Silicon-On-Insulator (SOI) CMOS technology
- RHA Total Ionizing Dose (TID)
  - 100 krad(Si) High Dose Rate
- Single-Event Effect (SEE) hardness
  - SET, SEFI, SEB and SEL characterized up to 67.7 MeV-cm^2/mg
- MIL-PRF-38535 compliant
- 1.8V, 2.5V and 3.3V compatible digital I/O
- Extended temperature range with optional burn-in

PIN CONFIGURATION



24-Pin Ceramic SOIC

PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION	
1	BUSA	analog output	MIL-STD-1553 bus driver A, positive signal	
2	$\overline{\text{BUSA}}$	analog output	MIL-STD-1553 bus driver A, negative signal	
3	RXENA	digital input	Receiver A enable. If low, forces RXA and $\overline{\text{RXA}}$ low	Internal pull-up resistor
4	RXA	digital output	Receiver A output, non-inverted	
5	$\overline{\text{RXA}}$	digital output	Receiver A output, inverted	
6	VDDIO	power supply	Power for digital I/O. Supports 1.8V, 2.5V or 3.3V.	
7	GNDIO	power supply	Ground for VDDIO supply	
8	$\overline{\text{RXB}}$	digital output	Receiver B output, inverted	
9	RXB	digital output	Receiver B output, non-inverted	
10	RXENB	digital input	Receiver B enable. If low, forces RXB and $\overline{\text{RXB}}$ low	Internal pull-up resistor
11	$\overline{\text{BUSB}}$	analog output	MIL-STD-1553 bus driver B, negative signal	
12	BUSB	analog output	MIL-STD-1553 bus driver B, positive signal	
13	VDDB	power supply	+3.3 volt power for transceiver B	
14	VDDB	power supply	+3.3 volt power for transceiver B	
15	TXINHB	digital input	Transmit inhibit, bus B. If high BUSB, $\overline{\text{BUSB}}$ disabled.	Internal pull-down resistor
16	TXB	digital input	Transmitter B digital data input, non-inverted	Internal pull-down resistor
17	$\overline{\text{TXB}}$	digital input	Transmitter B digital data input, inverted	Internal pull-down resistor
18	GND1P8	power supply	Ground for VDD1P8 supply	
19	VDD1P8	power supply	Power for 1.8V digital core	
20	$\overline{\text{TXA}}$	digital input	Transmitter A digital data input, inverted	Internal pull-down resistor
21	TXA	digital input	Transmitter A digital data input, non-inverted	Internal pull-down resistor
22	TXINHA	digital input	Transmit inhibit, bus A. If high BUSA, $\overline{\text{BUSA}}$ disabled.	Internal pull-down resistor
23	VDDA	power supply	+3.3 volt power for transceiver A	
24	VDDA	power supply	+3.3 volt power for transceiver A	

Table 1. Pin Descriptions

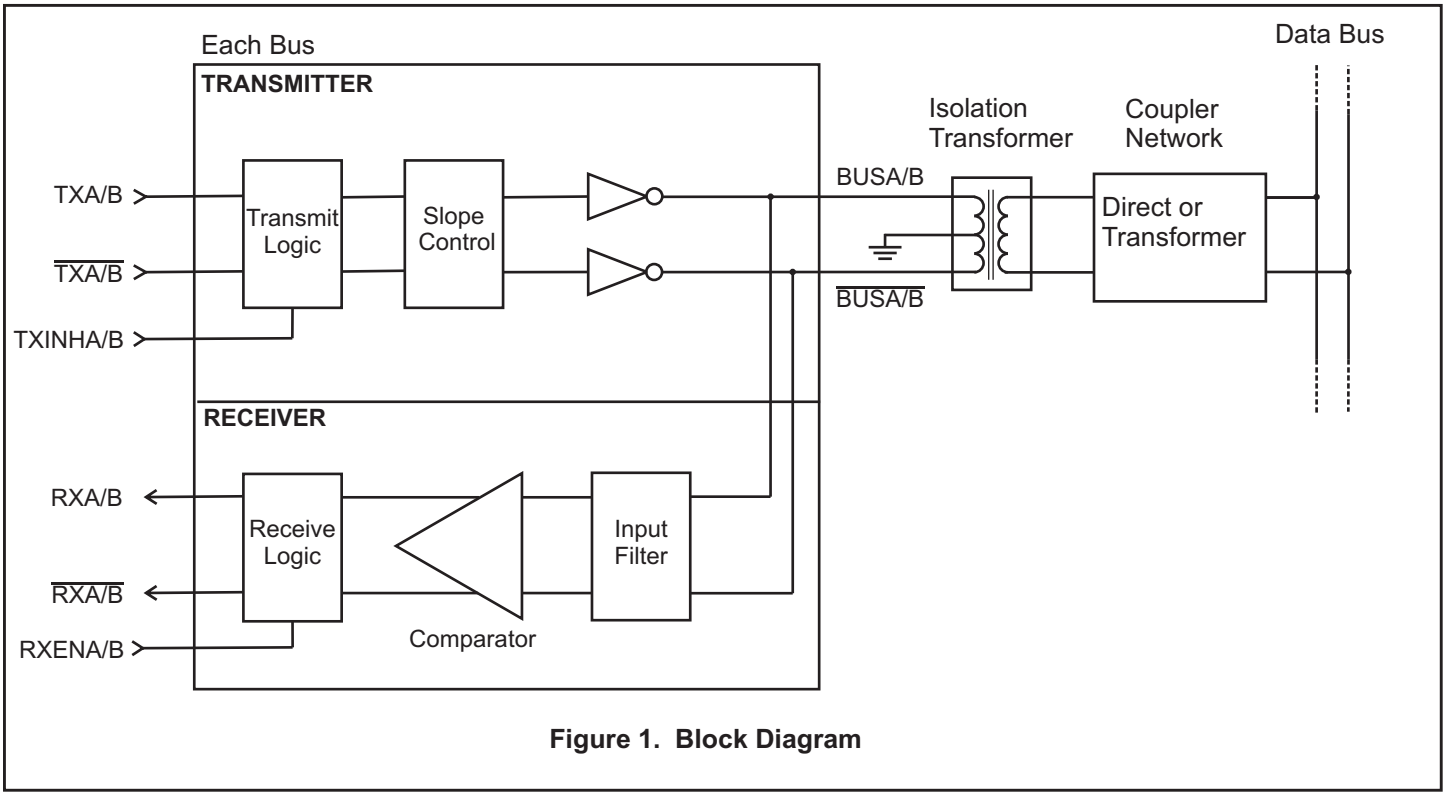
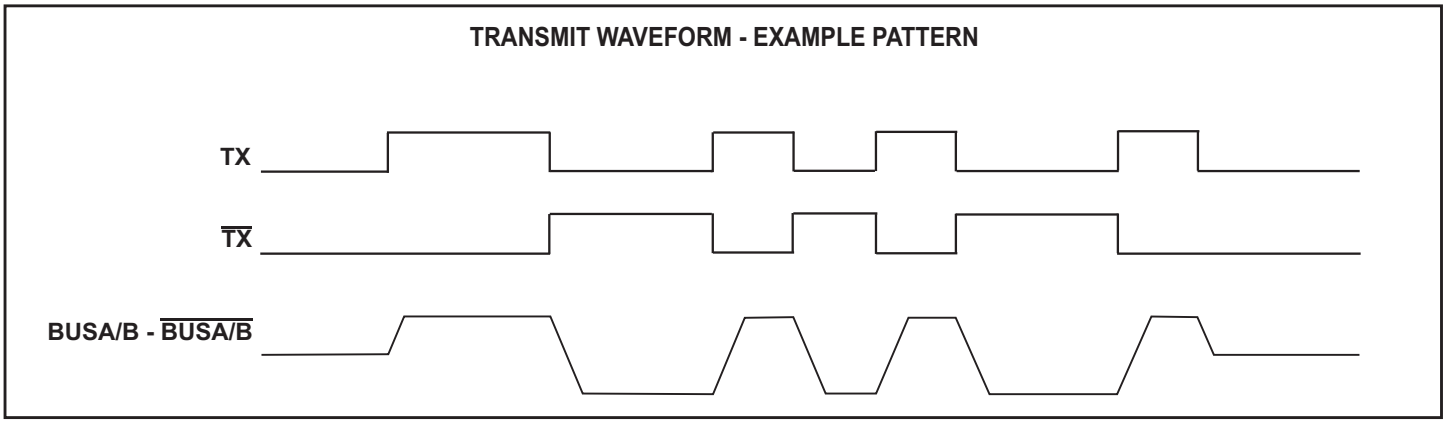
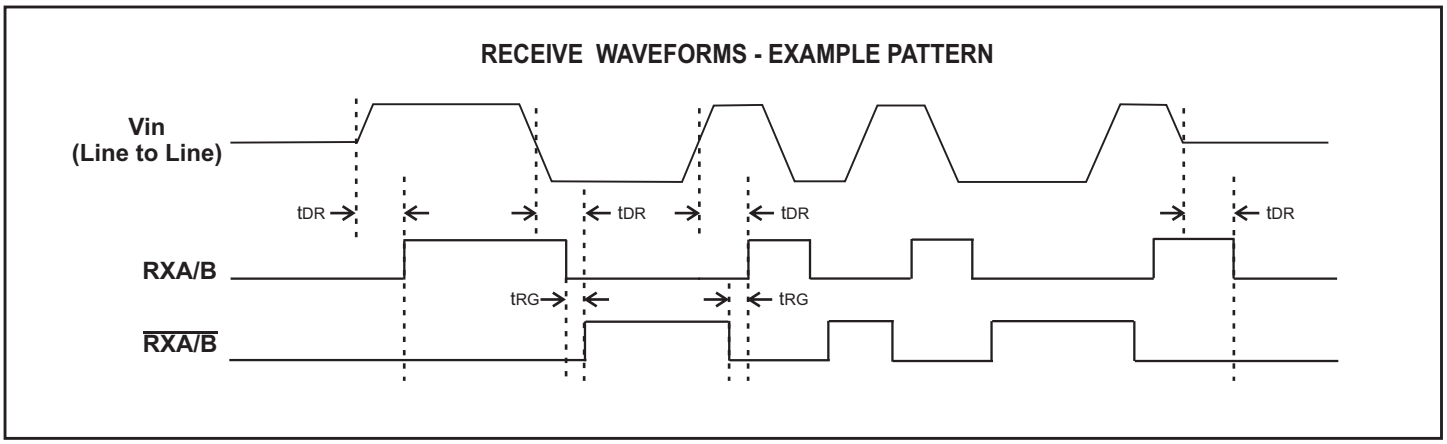


Figure 1. Block Diagram





FUNCTIONAL DESCRIPTION

The HI-1592 dual MIL-STD-1553 bus transceiver contains a differential voltage source driver and a differential analog bus receiver for each bus. It is designed for applications using a MIL-STD-1553B communications bus. The device generates a trapezoidal output waveform during transmission.

TRANSMITTER

Data input to the HI-1592 transmitter is a pair of complementary CMOS inputs TXA/B and $\overline{\text{TXA/B}}$. The transmitter accepts Manchester II bi-phase data and converts it to differential analog voltages on BUSA and $\overline{\text{BUSA}}$, or BUSB and $\overline{\text{BUSB}}$ The transceiver outputs are either direct- or transformer-coupled to the MIL-STD-1553 data bus. Both coupling methods produce a nominal voltage on the bus of 7.5 Volts peak to peak.

The transmitter is automatically inhibited and placed in the high impedance state when TXA/B and $\overline{\text{TXA/B}}$ are both driven to the same logic state. A bus transmitter is also forced to the high impedance state when logic "1" is applied at the TXINHA (or TXINHB) transmit inhibit input, regardless of the TXA/B and $\overline{\text{TXA/B}}$ input condition.

RECEIVER

The receiver accepts bi-phase differential analog signals from the MIL-STD-1553 bus through the same direct- or transformer-coupled interface at the BUSA and $\overline{\text{BUSA}}$ (or BUSB and $\overline{\text{BUSB}}$) pins. The receiver differential input stage drives a filter and threshold comparator to produce CMOS data at the RXA and $\overline{\text{RXA}}$ (or RXB and $\overline{\text{RXB}}$) output pins.

MIL-STD-1553 BUS INTERFACE

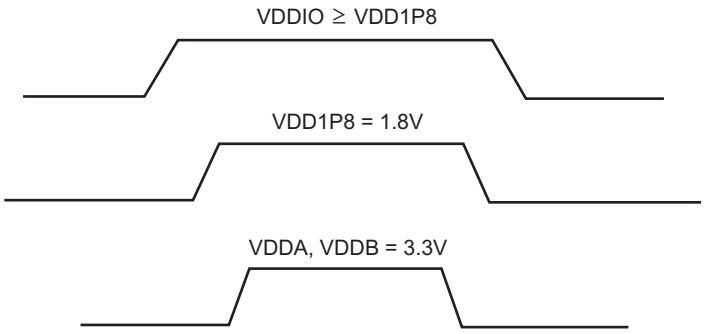
A direct-coupled interface (see Figure 2) uses a 1:2.65 turns-ratio isolation transformer and two 55 ohm isolation resistors between the transformer and the bus. The primary center-tap of the isolation transformer must be connected to GND.

In a transformer-coupled interface (see Figure 2), the transceiver is connected to a 1:2.5 turns-ratio isolation transformer which is connected to the main bus using a 1:1.4 turns-ratio coupling transformer. The transformer coupled method also requires two coupling resistors equal to 75% of the bus characteristic impedance (Zo) between the coupling transformer and the bus.

Figure 3 and Figure 4 show test circuits for measuring electrical characteristics of both direct- and transformer-coupled interfaces respectively. (See electrical characteristics on the following pages).

Power Sequencing

To prevent excessive current during power-on and power-off, it is recommended to power up VDDIO first, followed by VDD1P8 and finally VDDA, VDDB. This guarantees that the Line Driver inputs are in the correct state during power-up transients. For proper operation, VDDIO $\geq$ VDD1P8.



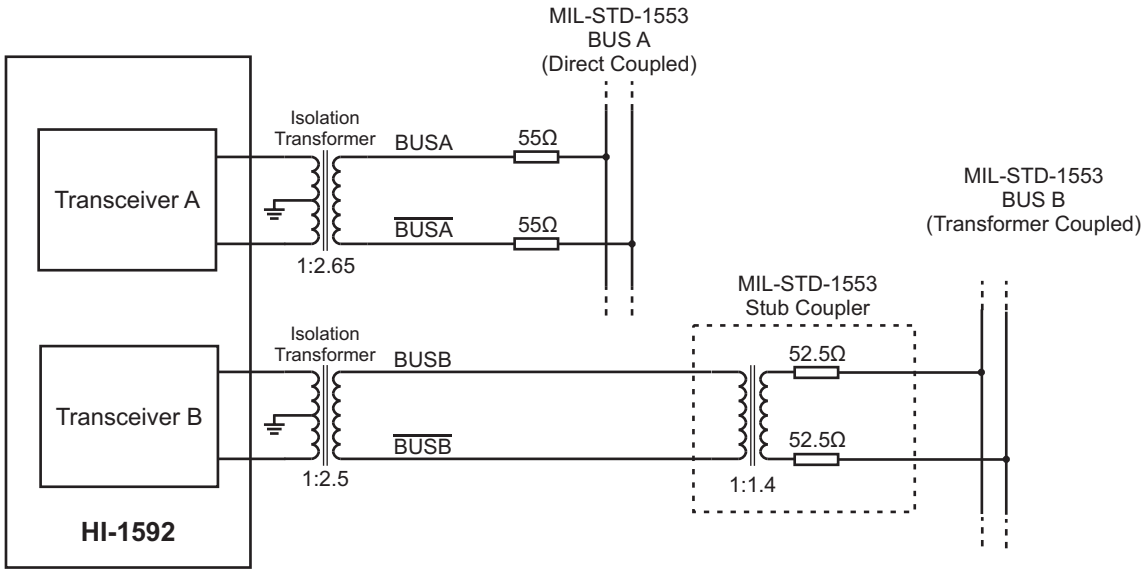


Figure 2. Bus Connection Example

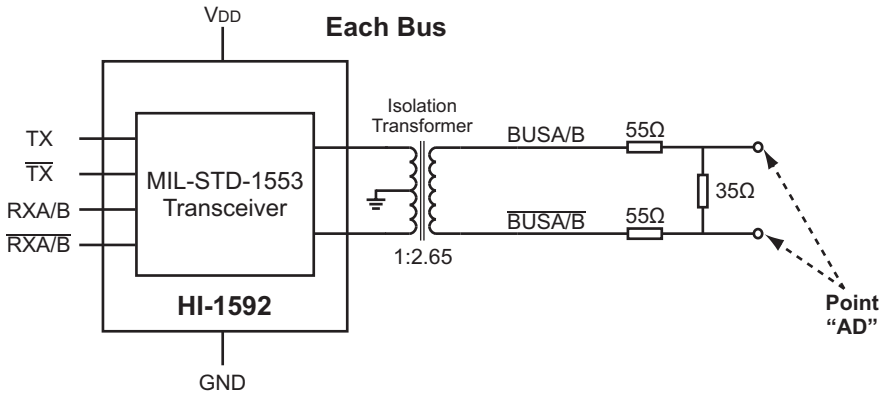


Figure 3. Direct Coupled Test Circuit

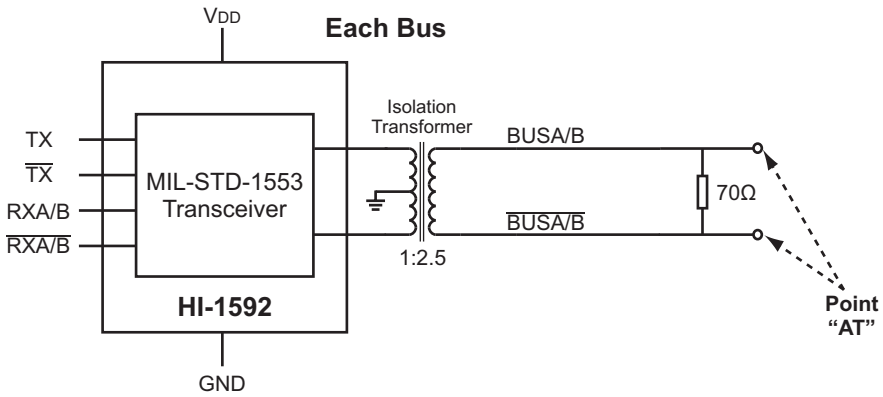


Figure 4. Transformer Coupled Test Circuit

ABSOLUTE MAXIMUM RATINGS

Supply voltages ($V_{DD}A$ or $V_{DD}B$)	-0.3 V to +5 V
Logic input voltage range	-0.3 V dc to +3.6 V
Voltage at BUSA/B or $\overline{BUSA/B}$ pins	+/-7 V
$V_{DDIO} - V_{DD1P8}$	0.5V
Reflow Solder Temperature	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages

V_{DDA} or V_{DDB} ..... 3.3V... ±5%
V_{DDIO} ..... 1.8V to 3.3V ± 10%
V_{DD1P8} ..... 1.8V... ±10%
$V_{DDIO} \geq V_{DD1P8}$

Temperature Range

Industrial ..... -40°C to +85°C
Hi-Temp ..... -55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

V_{DDA}, V_{DDB} = 3.15 V to 3.45V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Transceiver Supply Voltages	V_{DD}		3.14	3.30	3.46	V
Total Supply Current	I_{CC1}	Not Transmitting			420	µA
	I_{CC2}	Transmit one bus @ 50% duty cycle, 78 Ω resistive load		380	410	mA
	I_{CC3}	Transmit one bus @ 100% duty cycle, 78 Ω resistive load		700	750	mA
Power Dissipation	PD_1	Not Transmitting			1.5	mW
	PD_2	Transmit one bus @ 100% duty cycle, 78 Ω resistive load		1.0	1.2	W
Logic Supply Voltage	V_{DD1P8}		1.65	1.80	1.95	V
Logic Supply Current	I_{DD1P8}				10.0	mA
Digital I/O Supply Voltage	V_{DDIO}	1.8V Digital I/O	1.65	1.80	1.95	V
		2.5V Digital I/O	2.3	2.5	2.7	V
		3.3V Digital I/O	3.0	3.3	3.6	V
Digital I/O Supply Current	I_{DDIO}	Not Transmitting			350	µA
Min. Input Voltage (High)	V_{IH}	Digital inputs, $V_{DDIO} = V_{DD} = 3.3V$	70%			V_{DD}
Max. Input Voltage (Low)	V_{IL}	Digital inputs, $V_{DDIO} = V_{DD} = 3.3V$			30%	V_{DD}
Min. Output Voltage (High)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs $V_{DDIO} = V_{DD} = 3.3V$	90%			V_{DD}
Max. Output Voltage (Low)	V_{OL}	I_{OUT} = 1.0mA, Digital outputs $V_{DDIO} = V_{DD} = 3.3V$			10%	V_{DD}
Min. Input Voltage (High)	V_{IH}	Digital inputs, V_{DDIO} = 2.5V, V_{DD} = 3.3V	1.7			V
Max. Input Voltage (Low)	V_{IL}	Digital inputs, V_{DDIO} = 2.5V, V_{DD} = 3.3V			0.7	V
Min. Output Voltage (High)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs V_{DDIO} = 2.5V, V_{DD} = 3.3V	2.3			V
Max. Output Voltage (Low)	V_{OL}	I_{OUT} = 1.0mA, Digital outputs V_{DDIO} = 2.5V, V_{DD} = 3.3V			0.2	V

DC ELECTRICAL CHARACTERISTICS (cont.)

V_{DDA}, V_{DDB} = 3.15 V to 3.45V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Min. Input Voltage (High)	V_{IH}	Digital inputs, V_{DDIO} = 1.8V, V_{DD} = 3.3V	1.17			V
Max. Input Voltage (Low)	V_{IL}	Digital inputs, V_{DDIO} = 1.8V, V_{DD} = 3.3V			0.63	V
Min. Output Voltage (High)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs V_{DDIO} = 1.8V, V_{DD} = 3.3V	1.35			V
Max. Output Voltage (Low)	V_{OL}	I_{OUT} = 1.0mA, Digital outputs V_{DDIO} = 1.8V, V_{DD} = 3.3V			0.45	V
Min. Input Current (High)	I_{IH}	Digital inputs, V_{DDIO} = 3.6V			50	µA
Max. Input Current (Low)	I_{IL}	Digital inputs, V_{DDIO} = 3.6V	-50			µA
RECEIVER(Measured at Point "A_D" in Figure 3 unless otherwise specified)						
Input resistance	R_{IN}	Differential (at chip pins)	5			kOhm
Input capacitance	C_{IN}	Differential			5	pF
Input common mode voltage	V_{ICM}		-10.0		10.0	V-pk
Threshold Voltage - Direct-coupled Detect	V_{THD}	1 MHZ Trapezoidal Waveform Measured at Point "A_D" in Figure 3 RXA/B, $\overline{RXA/B}$ pulse width > 85 ns	1.15			Vp-p
No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$			0.28	Vp-p
Theshold Voltage - Transformer-coupled Detect	V_{THD}	1 MHZ Trapezoidal Waveform Measured at Point "A_T" in Figure 4 RXA/B, $\overline{RXA/B}$ pulse width > 85 ns	0.75			Vp-p
No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$			0.325	Vp-p
TRANSMITTER(Measured at Point "A_D" in Figure 3 unless otherwise specified)						
Output Voltage Direct coupled	V_{OUT}	35 ohm load (Measured at Point "A_D" in Figure 3)	6.0		9.0	Vp-p
Transformer coupled	V_{OUT}	70 ohm load (Measured at Point "A_T" in Figure 4)	18.0		27.0	Vp-p
Output Noise	V_{ON}	Differential, inhibited			10.0	mVp-p
Output Dynamic Offset Voltage Direct coupled	V_{DYN}	35 ohm load (Measured at Point "A_D" in Figure 3)	-90		90	mV
Transformer coupled	V_{DYN}	70 ohm load (Measured at Point "A_T" in Figure 4)	-250		250	mV
Output Capacitance	C_{OUT}	1 MHz sine wave			15	pF

AC ELECTRICAL CHARACTERISTICS

V_{DDA}, V_{DDB} = 3.15 V to 3.45 V, GND = 0V, T_A =Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER (Measured at Point "AT" in Figure 4 unless otherwise specified)						
Receiver Delay	t_{DR}	From input zero crossing to RXA/B or $\overline{RXA/B}$			450	ns
Receiver gap time	t_{RG}	Spacing between RXA/B and $\overline{RXA/B}$ pulses. 1 MHz sine wave applied at point "AT" Figure 4, amplitude range 0.86 Vp-p to 27.0Vp-p	90		365	ns
Receiver Enable Delay	t_{REN}	From RXENA/B rising or falling edge to RXA/B or $\overline{RXA/B}$			40	ns
TRANSMITTER (Measured at Point "AT" in Figure 4)						
Driver Delay	t_{DT}	TXA/B, $\overline{TXA/B}$ to BUSA/BUSB, $\overline{BUSA/BUSB}$			150	ns
Rise time	tr	70 ohm load	100	150	300	ns
Fall Time	tf	70 ohm load	100	150	300	ns
Inhibit Delay	t_{DI-H}	Inhibited output			100	ns
	t_{DI-L}	Active output			150	ns

ORDERING INFORMATION

HI - 1592CS x

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	MIL-PRF-38535 COMPLIANT	100% PIND	LEAD FINISH
T	-55°C TO +125°C	T	NO	NO	NO	Gold (Pb-free, RoHS compliant)
D	-55°C TO +125°C	D	YES	YES, QML-Q	YES	Tin / Lead (Sn63 / Pb37) Solder

Note: For additional screening options, contact the factory.

PART NUMBER	PACKAGE DESCRIPTION
1592CS	24 PIN CERAMIC WIDE BODY SOIC (24CSO)

RECOMMENDED TRANSFORMERS

The HI-1592 transceiver has been characterized for compliance with the electrical requirements of MIL-STD-1553 when used with the following transformers. Holt recommends Premier Magnetics parts as offering the best combination of electrical performance, low cost and small footprint.

MANUFACTURER	PART NUMBER	APPLICATION	TURNS RATIO	DIMENSIONS
Premier Magnetics	PM-DB2791S	Isolation	1:2.5	.400 x .400 x .185 inches
Premier Magnetics	PM-DB2796S	Isolation	1:2.65	.400 x .400 x .185 inches
Premier Magnetics	PM-DB2702	Stub coupling	1:1.4	.625 x .625 x .250 inches

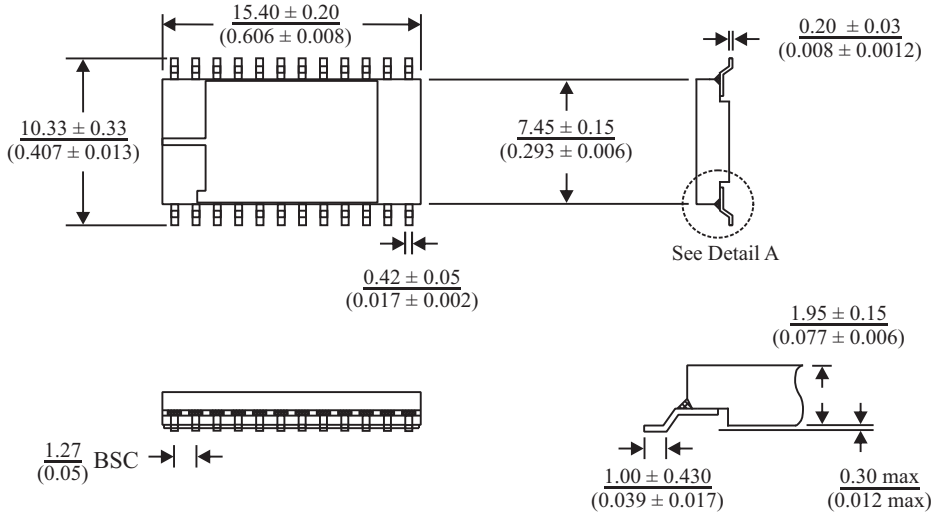
REVISION HISTORY

Document	Rev.	Date	Description of Change
DS1592	New	08/22/2024	Initial Release.

24-PIN CERAMIC SMALL OUTLINE (SOIC) - WB
(Wide Body)

millimeters(inches)

Package Type: 24CSO



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

Detail A